天鈺科技股份有限公司
Eureka Microelectronics,Inc.

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Eureka Microelectronics, Inc.

EK7307

OBJECTIVE

DATA SHEET

240-Output TFT Gate Driver IC

6F, NO.12, INNOVATION 1ST. RD.,
SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU CITY, TAIWAN, R.O.C.
TEL：886-3-5799255
FAX：886-3-5799253

240- Output TFT Gate Driver IC

DESCRIPTION

The EK7307 is a 240-output TFT gate driver IC suitable for driving large/medium scale of TFT LCD panels. The special, COG and COF compatible, pad layout allows direct mounting on the glass. The logic inputs, the logic outputs and the power supply pins are available on both sides and suitable for connecting multiple chips using the on chip connection as signal path.

FEATURES

- Output channels: 240 outputs
- Driver operating frequency: max. 1.2MHz
- LCD supply voltage: max. VEE+43V
- Driver output levels: two
- Driver "L" level is changeable
- Incorporates bi-directional shift register.
- Supports multi chip operation via output pins.
- Pulse width modulation function.
- COG and COF compatible pad layout
- Power and logic I/O pins on both sides
- Through Chip connection

BLOCK DIAGRAM

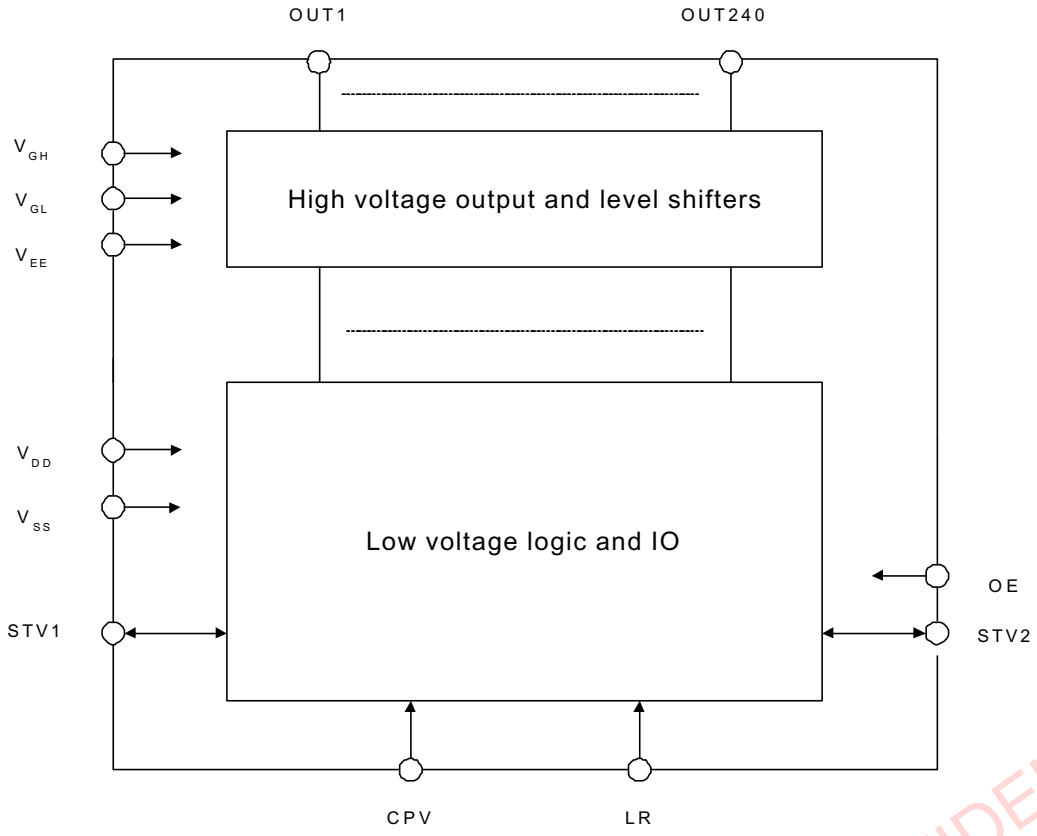

Fig. 1 Block diagram

PINNING INFORMATION

Table 1. Pad description

PAD Nr.	SYMBOL	I/O	Function	DESCRIPTION		
53 to 292	OUT_1 - OUT_{240}	O	TFT gate driver output	Under the control of the shift register data, OE, and STV1 or STV2, the driver outputs are V_{GH} or V_{GL} and change their value at the rising edge of CPV		
13 to 18, 327 to 332	V_{GL}		Supply	Power supply for TFT driver output low level		
7 to 12, 333 to 338,	V_{EE}		Supply	Negative power supply for Level shifters. Chip ground		
346 to 349, 467 to 470	V_{SS}		Supply	Logic ground, Reference of the voltages		
31 to 33, 38 to 41, 304 to 307 312 to 314	LR	I	Shift direction selection signal	LR = "H" : OUT1 → OUT240 (Shift left) LR = "L" : OUT240 → OUT1 (Shift right)		
25 to 27 318 to 320	STV1	I/O	Start pulse input and output		**STV1**	**STV2**
28 to 30 315 to 317	STV2			LR = "H"	Input	Output
				LR = "L"	Output	Input
34 to 37 308 to 311	CPV	I	Shift register clock input	The start pulse is sampled at the rising edge of CPV, The carry pulse changes at the falling edge of CPV.		
42 to 45 300 to 303	OE	I	Negative active input pin	When OE = "H" then the outputs are set to V_{GL} independent of the register data. This function is not synchronized with CPV.		
1 to 6 339 to 344 350 to 355 461 to 466	V_{DD}		Supply	Logic positive power		
19 to 24 321 to 326 356 to 361 455 to 460	V_{GH}		Supply	High voltage power and TFT driver output high level		

FUNCTIONAL DESCRIPTION

Power supplies

The TFT voltage, V_{GL} and V_{EE}, relative to the logic ground, can be a negative voltage value.

The TFT gate driver pins are either V_{GL} or V_{GH}.

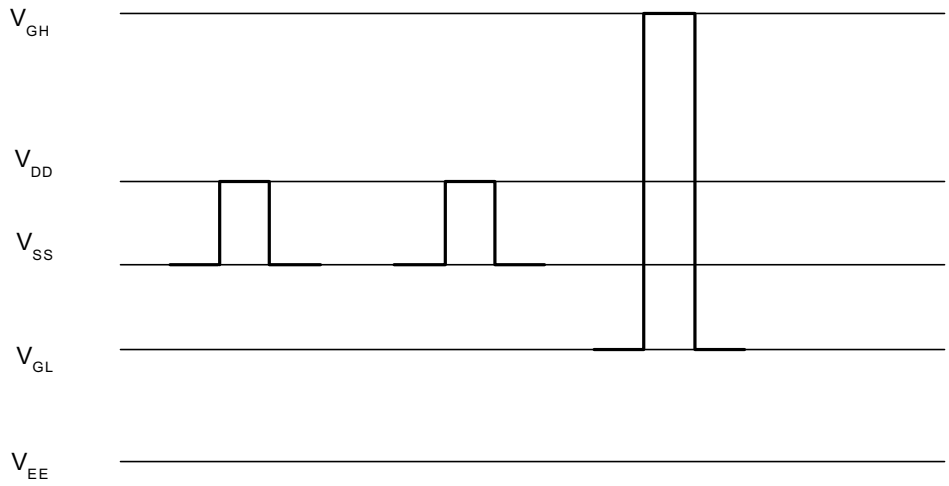

Fig. 2 Relative position of the different supply voltages

Shift direction

The input signals OE and the shift data control the value of the outputs (OUT_1 till OUT_{240}). Their value can be either V_{GH} or V_{GL}.

The signal LR controls the shift direction of the shift register. The shift register takes its value from one of the input/output pins STV at the rising edge of the clock CPV and shifts the value to the other input/output pin STV where it is presented at the falling edge of CPV.

Table 2. LR shift direction relation

LR	Start pulse taken from:	Data shift direction	Output pulse given at:
LR="H"	STV1	$OUT_1 \rightarrow OUT_{240}$	STV2
LR="L"	STV2	$OUT_{240} \rightarrow OUT_1$	STV1

OE function

When the OE input is “H” than the outputs are driven to V_{GL} regardless of the contents of the shift register. This function is not synchronized with CPV.

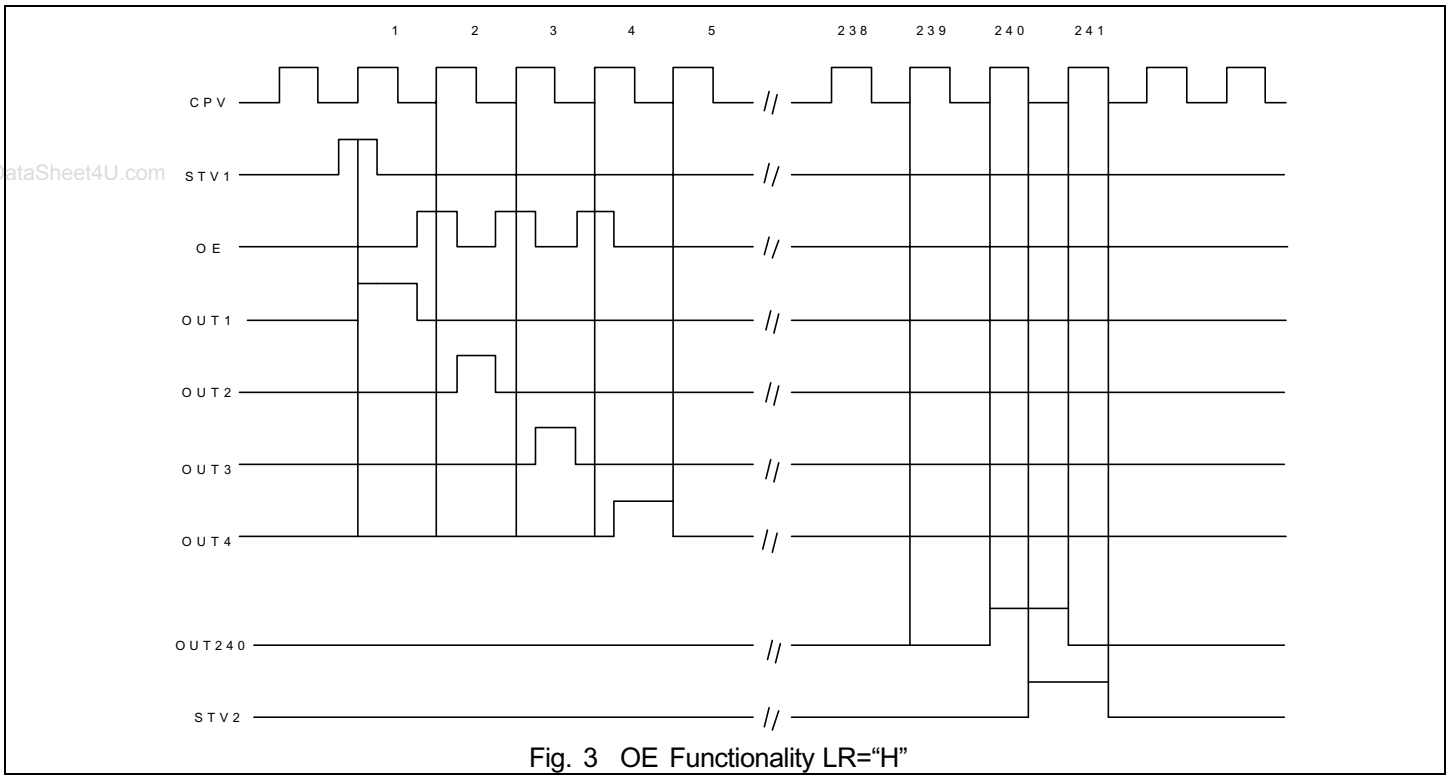

Fig. 3 OE Functionality LR=“H”

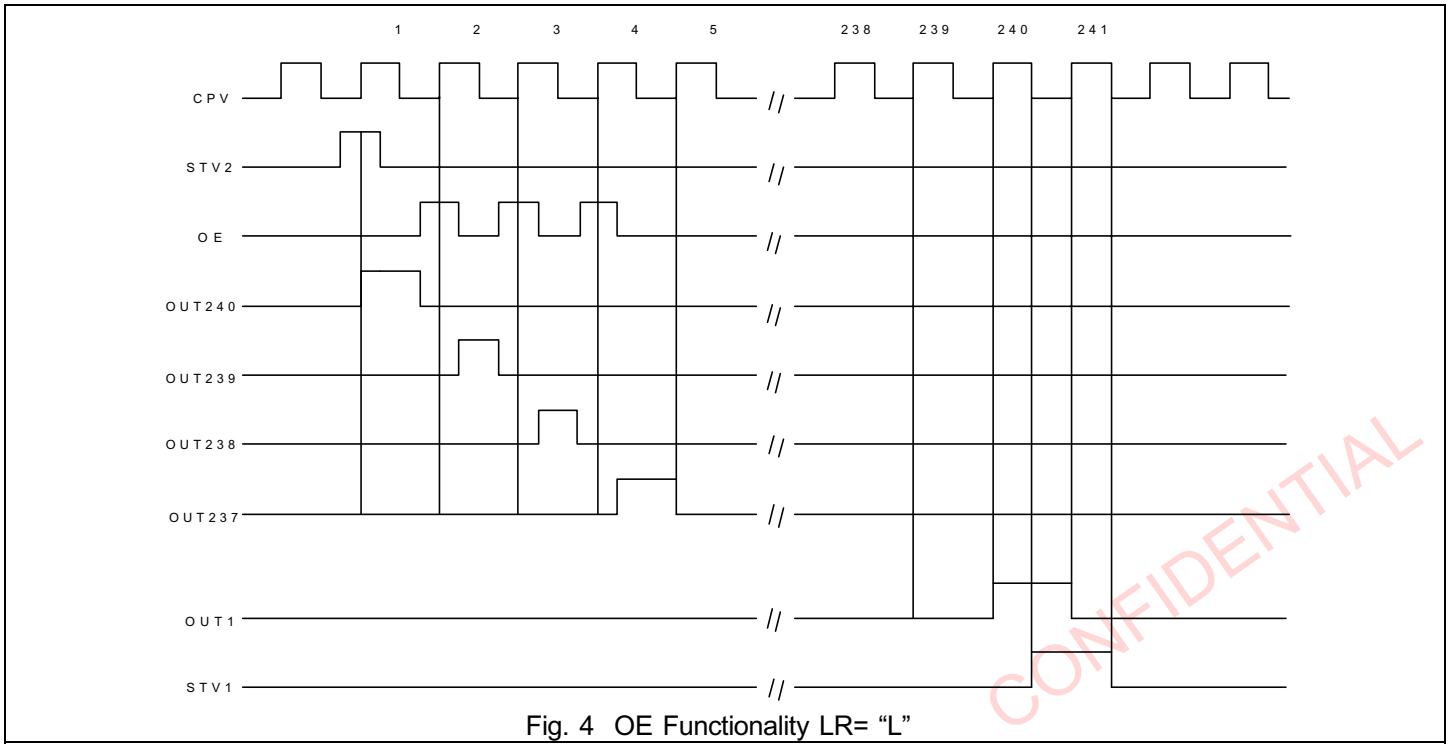

Fig. 4 OE Functionality LR= “L”

CIRCUIT DIAGRAMS

Input/Output Circuit

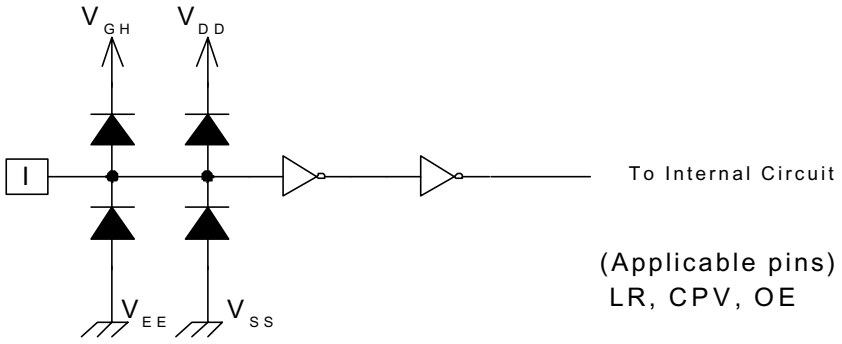

Fig. 5 Input Circuit

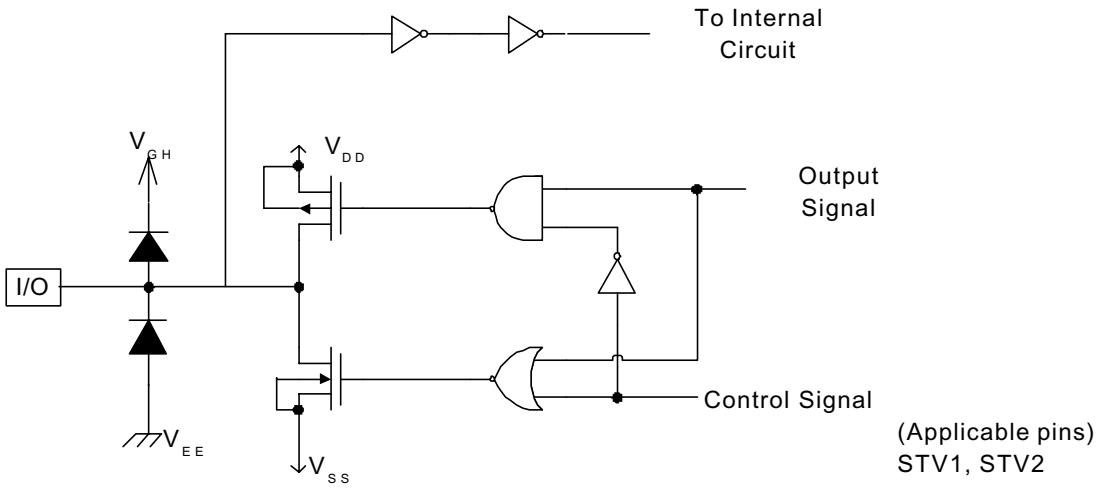

Fig. 6 Input/Output Circuit

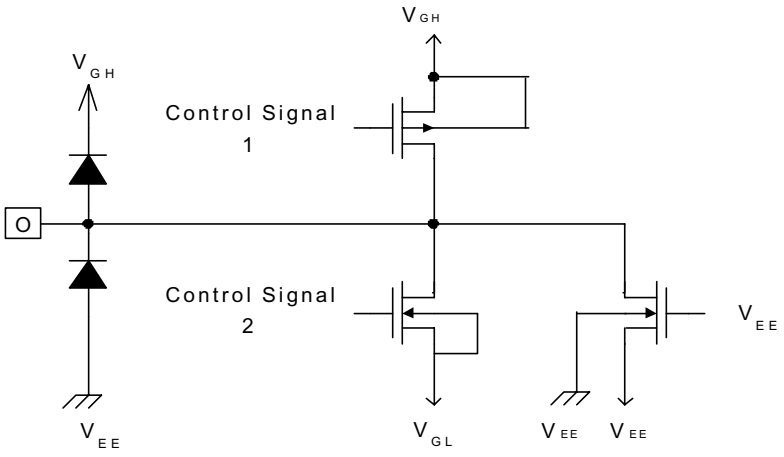

Fig. 7 TFT driver circuit

PRECAUTIONS

Precaution when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow, if voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute maximum Ratings

In accordance with the Absolute Maximum Ratings System (IEC 134); See notes 1 and 2

Parameter	Symbol	Applicable Pins	Ratings	Unit	Notes
Supply voltage(1)	V_{DD}	V_{DD}	V_{SS} -0.3 to V_{SS}+7.0	V	1, 2
Supply voltage(2)	V_{GH}	V_{GH}	V_{EE} -0.3 to V_{EE}+45.0	V	
	V_{EE}	V_{EE}	V_{GH} -45 to V_{GH}+0.3	V	
	V_{GL}	V_{GL}	V_{EE} -0.3 to V_{GH}+0.3 V_{EE} -0.3 to V_{EE}+7	V	
	V_{DD}	V_{DD}	V_{EE} -0.3 to V_{EE}+45.0	V	
	V_{SS}	V_{SS}	V_{EE} -0.3 to V_{GH}+0.3	V	
Input voltage	V_I	OE, STV1 STV2, LR, CPV	V_{SS} -0.3 to V_{DD}+0.3 V_{EE} -0.3 to V_{GH}+0.3	V	
Storage temperature	T_{stg}		-45 to +125	℃	

Notes:

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device
2. Parameters are valid over operating temperature range unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Table 4. Recommended operating conditions

Parameter	Symbol	Applicable pins	Min.	Typ.	Max.	Unit	Notes
Supply voltage(1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage(2)	V_{GH}	V_{GH}	+10.0		+42.0	V	
Supply voltage(3)	V_{EE}	V_{EE}	-25		-5	V	
Supply voltage(4)	V_{GL}	V_{GL}	V_{EE}		V_{EE}+5	V	
Operating temperature	T_{OPR}		-20		+75	℃	

Notes:

1. All voltages are with respect to V_{SS} unless otherwise noted (0 V).
2. Ensure that voltages are set such that $V_{EE} \le V_{SS} < V_{DD}$, $V_{EE} \le V_{SS} < V_{GH}$ and $V_{EE} \le V_{GL} < V_{GH}$

ELECTRICAL CHARACTERISTICS

Table 1. DC Characteristics

(V_{SS}=0 V, V_{DD}=+2.5V to +5.5V, V_{GH}=+15.0 to +42.0 V, T_{OPR}=-20 to +75℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit	Note
Operating Supply Current	IDD	fCPV=15.7kHz fSTV=60Hz V_{DD}=3.3V V_{EE}=-15V V_{GH}=15V Output with no load	VDD			800	μA	
Operating Supply Current	IGH		VGH			300	μA	
Standby quiescent Supply Current	IDS	Standby V_{DD}=3.3V V_{EE}=-15V V_{GG}=15V	VDD			600	μA	
Standby quiescent Supply Current	IGS		VGH			100	μA	
Input pin								
H input voltage	VIH1		LR, CPV, OE	0.8xVDD		VDD	V	
L input voltage	VIL1			0		0.2xVDD	V	
Input leakage current	VLI1			-10		10	μA	
Input/Output pin								
H input voltage	VIH3		STV1, STV2	0.8xVDD		VDD	V	
L input voltage	VIL3					0.2xVDD	V	
H output voltage	VOH	I_O = -100 μA		VDD-0.4			V	
L output voltage	VOL	I_O = 100 μA				0.4	V	
Liquid crystal driving voltage input pin								
Input leakage current	VLI2	Out1 ~ Out240 = High	VGL	-100		100	μA	
Liquid crystal driving voltage output pin								
Output leakage current	VLO1		OUT1 to OUT240	-50		50	μA	
Output ON resistance	RON-VGH	V_{GH}=15V V_{EE}=-15V V_{OM}=VGH-0.5V V_{OM} is OUT1~OUT240			600	1000	Ω	
	RON-VGL	V_{GH}=15V V_{EE}=-15V V_{GL}=-10v V_{OM}=V_{GL}+0.5V V_{OM} is OUT1~OUT240			600	1000	Ω	

Table 6. AC Characteristics

(V_{SS}= 0 V, V_{DD}=+2.5V to +5.5V, V_{GH}-V_{EE}=+30.0 to +42.0 V, T_{OPR}=-20 to +75℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock period	t_{CPV}		833			ns
Pulse width of clock H level	t_{WH}		350			ns
Pulse width of clock L level	t_{WL}		350			ns
STV data set up time	t_{SU}		50			ns
STV data hold time	t_H		350			ns
STV output delay time	tpd1	CL=50pF			300	ns
OUT 1 to 240 output delay time	tpd2	CL=300pF			800	ns

Timing Chart

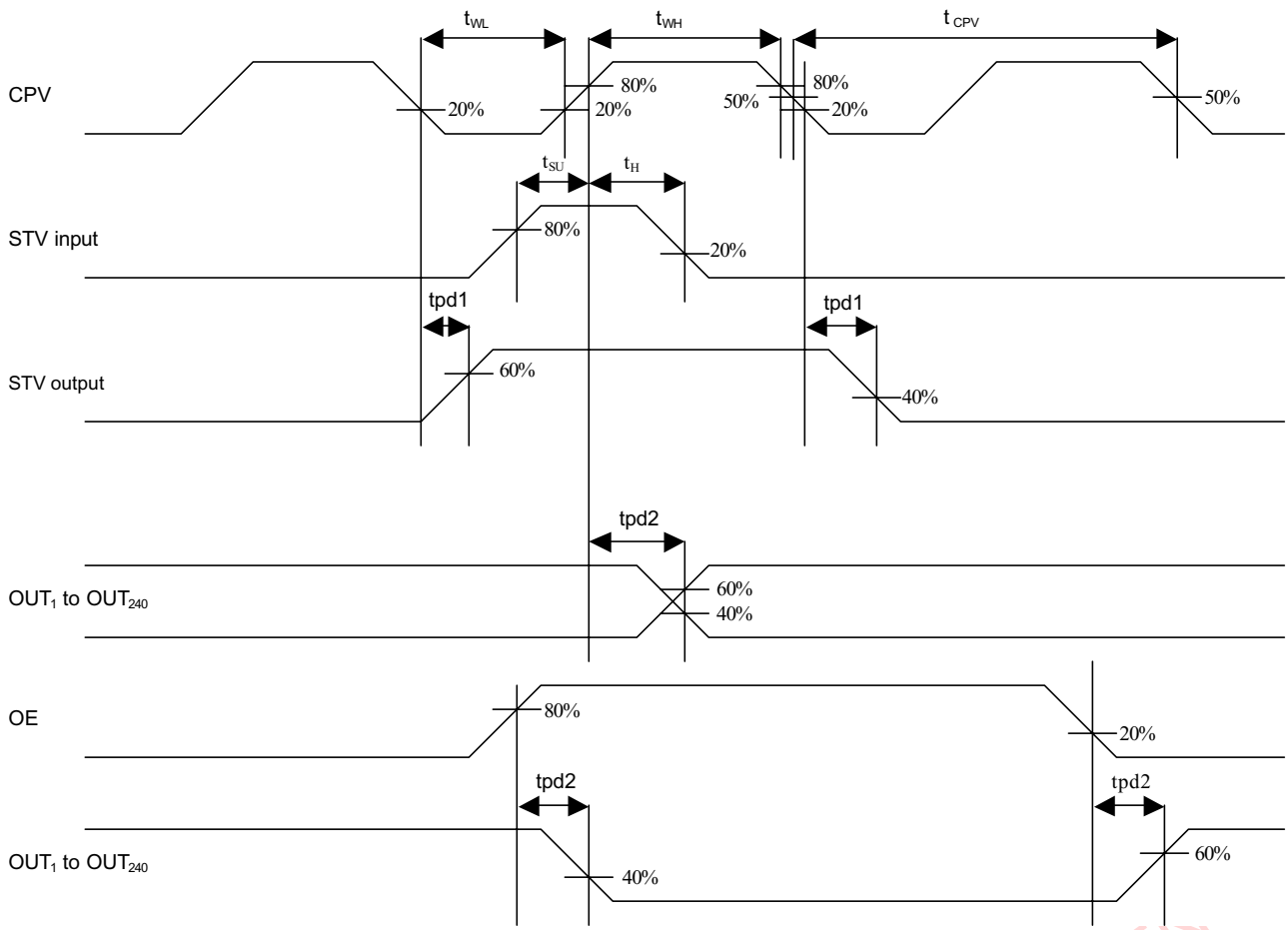

Fig. 8 Timing

DEFINITIONS

Data Sheet status	
Objective specification	This data sheet contains target or goal specification for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specification.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Eureka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Eureka for any damages resulting from such improper use or sale.